

DECOUPLING CAPACITOR METHOD FOR A PHASE LOCKED LOOP

Abstract

A method for optimizing decoupling capacitance in a phase locked loop is provided. A representative power supply waveform having noise is input into a simulation of the phase locked loop; an estimate of jitter is determined; and an amount of the decoupling capacitance is adjusted until the jitter falls below a pre-selected value. Further, a computer system for optimizing decoupling capacitance in a phase locked loop is provided. Further, a computer-readable medium having recorded thereon instructions adapted to optimize decoupling capacitance in a phase locked loop is provided.

23885_1.DOC